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Inventor(s). INABA	142,264			Examiner: Atty. Dkt.	Dickey, Tho P 284163	omas L. 🧷 01F181	200
FF*KV******************************	94∠,∠04 Serial No. ↑			Ally. DKI.	M#	Client Ref	
Filed: January 11, 2002	,			Appln. Title:	SEMICONDUCT	COENTROL	-17
Hon. Commissioner of Patents					REALIZING CHA	ARAGIERIST	ICS FIKE
Washington, D.C. 20231					A SOI MOSFET		G.
•						更见	CENED
Sir:				D-4-	A	Œ	四四
REPLY/AMENDMENT/LETTER				Date:	REALIZING CHA A SOI MOSFET April 25, 2003	X.	CENED 2003
This is a reply/amendment/letter in the	e above-identi	fied application	on and	includes the here			
which is incorporated hereinto by refe	rence and the	signature be	elow is	treated as the sig	nature to the attacl	nment in abse	nce of a
signature thereto.		J				C	•
	FEE REQUI	REMENTS F	OR CL	<u>AIMS AS AMEN</u>	<u>DED</u>		
1. Small Entity claim							
A. NOT made For B & C	Claims remaining after	Highest nur previously pa		Present Extra	Large/Small Entity	Additional Fee	Fee Code
C. D made herewith Separate Paper	amendment	previously pr	210 101			'"	Lg/Sm
D. made previously (Pat-256)		,					
						ļ	100100
2. Total Effective Claims	46	**minus	46	0	x \$18/\$9 =	+ \$0	103/203
3. Independent Claims	10	***minus	10	0	x \$84/\$42 =	+ \$0	102/202
4. If amendment enters proper multip					+ \$280/\$140 =	+ \$0	104/204
time (leave blank if this is a reissue a				add	T \$200/\$140 -	- Φ0	104/204
5. Original due Date: April 30, 200		NONE /	1 mo)	\$110/\$55 =	T		115/215
6. Petition is hereby made to extend date to cover the date this response is			mos)	\$410/\$35 =	+ \$0		116/216
requisite fee is attached	S IIICU IOI WIIIC	•	mos)	\$930/\$465 =	" 🗸 "		117/217
requisite ice is attached		•	mos)	\$1,450/\$725=			118/218
		•	mos)	\$1,970/\$985=			128/228
7. Enter any previous extension fee p	aid since abov	e <u>original</u> du	e date	and <u>subtract</u>	- \$0		
8.					Extension Fee	+ \$0	
9. If Terminal Disclaimer attached, a					+ \$110/\$55	+ \$0	148/248
10. If IDS attached requires Official Fee under Rule 97 (c),				add	+ \$180	+ \$0	126 126
or if Rule 97(d) Request				add	+ \$180	. 60	146/246
*11. After-Final Request Fee per rules 129(a) and 17(r)					+ \$750/370	+ \$0	149/249
					x \$750/375 ea + \$750/375	+ \$0 + \$0	1179/1279
13. Request for Continued Examinated 14. Petition fee for	13. Request for Continued Examination (RCE)					+ \$0	
15. TOTAL FEE =						\$0	L
	16. *If the entry in this space is less than entry in next space, the "Present Extra" result is "0".						II A D C E
co the me entry in this snace is less than entry						PLEASE C OUR DEP.	
16. *If the entry in this space is less than entry 17. **If the "Highest number previously paid to			vrite "3"	in this space.		OUR DET.	ACCI
		is less than 3, v					
17. **If the "Highest number previously paid		is less than 3, v	Our	Deposit Account	No. 03-3975)		
17. **If the "Highest number previously paid		e is less than 3, v	Our	Deposit Account r Order No. <u>44</u> 0	No. 03-3975) 020 284163 C# M#		
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NOTE: File this cover sheet in duplicate with PTO receipt (PAT-103A) and attachments

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

re PATENT APPLICATION OF

Confirmation No.: 6258

INABA

Group Art Unit: 2826

Appln. No.: 10,042,264

Examiner: Dickey, Thomas L.

Filed: January 11, 2002

Title: SEMICONDUCTOR DEVICE REALIZING CHARACTERISTICS LÍĶE

MOSFET (As Amended)

April 25, 2003

Hon. Commissioner of Patents Washington, D.C. 20231

Sir:

In response to the Office Action dated January 30, 2003, please enter the following amendments and remarks:

IN THE TITLE:

Please replace the Title of the Disclosure with the following new Title:

SEMICONDUCTOR DEVICE REALIZING CHARACTERISTICS LIKE A SOI **MOSFET**

Please see the attached specification for the changes made to effect the title.

IN THE CLAIMS:

Please amend claim 1 as follows:

- (Amended) A semiconductor device comprising:
- a semiconductor substrate having a surface;
- a gate electrode formed over the surface of said semiconductor substrate with a gate dielectric film interposed therebetween;

a pair of source and drain diffusion layers formed in said semiconductor substrate to oppose each other with a channel region laterally residing therebetween at a location immediately beneath said gate electrode, said source and drain diffusion layers each having a low resistivity region and an extension region being formed to extend from this low resistivity

